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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,590	10/17/2003	Rung-Ji Shang	41144-8003US	2090

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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,590	SHANG, RUNG-JI	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8 and 9* is/are rejected.

7)☒ Claim(s) *3 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 10/17/2003 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Objections

4. Claims 1 and 6 are objected to because of the following informalities:

In claim 1, last line, "the cache memory" should be changed to -- the RAID cache memory--.

In claim 6, lines 2, "the cache memory" should be changed to -- the RAID cache memory--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the dirty buffers" in lines 2-4. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the least used buffer" in lines 4. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-7 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7of

copending Application No. 10/10/688,359. Although the conflicting claims are not identical, they are not patentably distinct from each other because an element "non-volatile random access memory" in the application 10/688,359 would have been obvious to one of ordinary skill in the art since the cache memory as claimed in the application 10/688,359 is the type of RAM and can be modify to non-volatile random access memory. The limitation "at predetermined events" in the application 10/688,590 would have been obvious to one of ordinary skill in the art since the predetermined events includes the event "when the RAID controller is idle" as claimed in the application 10/688,590.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-2,4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Butterworth et al., US 6,941,420 B2.

Regarding claim 1, Butterworth teaches that a RAID-5 (Fig.2) configured storage system comprising:

a RAID controller (array control unit 108 in Fig.2),

a non-volatile random access memory (NVRAM) serving as a RAID cache memory (118, col.5, lines 13-14),

a plurality of physical disks (106a-106d); and

at least one logical disk (it is taught as one segment or more segments, col.4, lines 43-44);

wherein said storage system is operative to:

(1) read data from said logical disk (col.4, lines 66 to col.5, lines 40);

(2) write data to said logical disk (col.4, lines 66 to col.5, lines 40 and col.6, lines 21-35);

(3) flush data from said RAID cache memory to said logical disk at predetermined events (col.7, lines 8-10); and

(4) otherwise perform read/write operations under the control of the RAID controller to the cache memory (col.5, lines 18-28 and lines 52-56).

Regarding claim 2, Butterworth teaches that the writing process comprises:

reading an old data block and an old parity block from said logical disk or said RAID cache (col.2, lines 22);

forming a new parity block and a new data block by computing an XOR with the new data and the old data block and the old parity block (col.2, lines 24-27);

updating the logical disk by placing the new data block and the new parity block in the RAID cache or the logical disk (col.2, lines 27-29).

Regarding claim 4, Butterworth teaches that the reading process comprises:

determining whether an old data block to be read is already stored in the RAID cache memory, and if so, reading said old data block from said RAID cache memory (col.5, lines 7-14); and

if said old data block is not stored in the RAID cache memory, allocating a read buffer area from said RAM cache memory and transferring said old data block from said logical disk to said read buffer area and reading said old data block from the RAID cache memory (col.5, lines 46-48, it is taught as allocating a clean LRU list specifies logical tracks containing information wherein the data in the LSA cache is the same as the data in the DASD array, then the data block can be read from the clean LRU list).

Regarding claim 5, Butterworth teaches that said read buffer area (it is taught as a clean LRU list) is a non-dirty and least used block within the RAID cache memory (col.5, lines 41-46).

Regarding claim 6, Butterworth teaches that flushing the cache memory comprises:

selecting the dirty buffers in the cache memory (col.5, lines 44-46);

writing the dirty buffers to the logical disk (co.5, lines 56-59); and

setting the dirty buffers as a clean buffer in the RAID cache memory (col.5, lines 59-61).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butterworth et al., US 6,941,420 B2, in view of Schumann., US 6,205,521 B1.

Regarding claim 8, Butterworth teaches the claimed invention as shown above, Butterworth does not teach that during start up of said system after power loss, the system performs mapping the entire NVRAM to said logical disk; checking whether a dirty flag for said NVRAM is on or off; and flushing all of the dirty blocks of said NVRAM to said logical disk and resetting the dirty flag to off.

However, Schumann teaches that mapping the entire NVRAM to said logical disk (col.4, lines 46-50 and col.6, lines 28-30); checking whether a dirty

flag for said NVRAM is on or off (col.6, lines 24-27) and flushing all of the dirty blocks of said NVRAM to said logical disk 34-45 (col.6, lines) and resetting the dirty flag to off (col.4, lines 39-41).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Schumann into Butterworth's system such as mapping the entire NVRAM to said logical disk; checking whether a dirty flag for said NVRAM is on or off; and flushing all of the dirty blocks of said NVRAM to said logical disk and resetting the dirty flag to off because a cache map will accelerates cache memory operations (col.1, lines 5-7) and flushing only the dirty blocks of a cache memory will preventing consume a significant portion of the total power dissipation of the system (col.1, lines 57-67 and col.2, lines 34-36).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 9, Butterworth teaches that during a shut down process: all dirty blocks of said NVRAM is flushed to said logical disk; and setting off a dirty flag of said NVRAM (Fig.3B and col.5, lines 31-52).

Allowable Subject Matter

13. Claims 3 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McKnight et al	US 6629211 B2
Buckland et al	US 6467022 B1
Yang et al	US 6243795 B1
Brant et al	US 6760807 B2

15. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

16. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

October 24, 2005

FOR
Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

GARY PORTKA
PRIMARY EXAMINER